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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/043,637 | 01/09/2002 | Arthur H. Khu | X-996 US | 6525 |

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XILINX, INC
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| EXAMINER | |
|---|---|
| THAI, XUAN MARIAN | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2111 | |

DATE MAILED: 07/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/043,637 | KHU ET AL. | |
| | Examiner | Art Unit | |
| | XUAN M. THAI | 2111 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This is in response to communication filed on January 9, 2002. Claims 1-21 are pending in the application.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 3-6 and 9-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Jeppesen, III et al. (USPN 5,708,773; Jeppesen).

As per claim 1, Jeppesen discloses a JTAG-compliant chip for communicating with a non-JTAG-compliant chip comprising: a JTAG-compliant test access port (TAP) controller (fig. 1B; TAP 12); a plurality of pins (fig. 1B) extending from the JTAG-compliant chip to the non-JTAG-compliant chip; and a controller (Fig. 1C) connected receive signals from a shift register (e.g. 17), and in response to the signals from the shift register and the TAP controller, send and receive signals on the plurality of pins extending from the JTAG-compliant chip to the non-JTAG-compliant chip (fig. 2B). See col. 8, line 58 to col. 11, line 24.

As per claim 3, Jeppesen discloses "wherein the TAP controller accesses external TDI and TDO control signals." See fig. 1A.

As per claim 4, Jeppesen discloses "wherein the TAP controller allows the controller to access the external TDI and TDO control signals." See fig. 1C.

As per claim 5, Jeppesen discloses "wherein the controller comprises: shift register connected to external TDI and TDO control signals; and a state machine that response to commands in the shift register sends and receives signals on the plurality of pins extending from the JTAG-compliant chip to the non-JTAG-compliant chip." See fig. 1C.

As per claim 6, Jeppesen discloses "wherein the controller uses the signals on the plurality of pins extending from the JTAG-compliant chip to the non-JTAG-compliant chip to write to and read from the non-JTAG-compliant chip." See col. 9, line 50 to col. 10, line 3.

As per claim 9, Jeppesen discloses a method of using a programmable chip having a boundary scan structure to access a chip not having a boundary scan structure comprising: programming the chip having the boundary scan structure to implement a controller for: receiving boundary scan input signals (col. 9, lines 14-23), providing boundary scan output signals (col. 9, lines 20-23 and 16-17 and 55-67), providing signals to the chip not having a boundary scan structure (col. 9, lines 20-23 and 16-17 and 55-67) , and receiving signals from the chip not having a boundary scan structure (col. 10, lines 1-3).

As per claim 10, Jeppesen discloses the method wherein the step of providing signals to the chip not having a boundary scan structure comprises providing commands indicate one of a plurality of operations be performed (e.g. col. 9, lines 30-64).

4. Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Lulla et al. (USPN 6,757,844; Lulla).

As per claim 1, Lulla discloses a JTAG-compliant chip for communicating with a non-JTAG-compliant chip comprising: a JTAG-compliant test access port (TAP) controller (col. 4, lines 62-64); a plurality of pins extending from the JTAG-compliant chip to the non-JTAG-compliant chip (col. 3, lines 3-4); and a controller connected to receive signals from a shift register, and in response to the signals from the shift register and the TAP controller, send and receive signals on the plurality of pins extending from the JTAG-compliant chip to the non-JTAG-compliant chip (e.g. col. 4, lines 38-61 and col. 5, lines 1-67).

As per claim 2, Lulla discloses wherein the JTAG-compliant chip is a programmable logic device and the controller configured from logic in the programmable logic device. See col. 1, lines 21-58).

As per claim 3, Lulla discloses "wherein the TAP controller accesses external TDI and TDO control signals." See col. 2, lines 60-67.

As per claim 4, Lulla discloses "wherein the TAP controller allows the controller to access the external TDI and TDO control signals." See col. 2, lines 60-67; col. 5, lines 7-15.

As per claim 5, Lulla discloses "wherein the controller comprises: shift register connected to external TDI and TDO control signals; and a state machine that response to commands in the shift register sends and receives signals on the plurality of pins extending from the JTAG-compliant chip to the non-JTAG-compliant chip." See e.g. fig. 8. col. 6, lines 37 et seq.

As per claim 6, Lulla discloses "wherein the controller uses the signals on the plurality of pins extending from the JTAG-compliant chip to the non-JTAG-compliant chip to write to and read from the non-JTAG-compliant chip." See e.g. col. 3, lines 21-24.

As per claim 7, Lulla discloses "wherein the non-JTAG-compliant chip is a flash memory chip and the controller further uses the signals on the plurality of pins extending from the JTAG-compliant chip to the non-JTAG-compliant chip to erase the flash memory chip." See e.g. col. 3, lines 21-24; col. 8, lines 43 et seq.

As per claim 8, Lulla discloses "wherein the programmable logic device is a field programmable gate array chip." See col. 1, lines 21-58.

As per claim 9, Lulla discloses a method of using a programmable chip having a boundary scan structure to access a chip not having a boundary scan structure comprising: programming the chip having the boundary scan structure to implement a controller for: receiving boundary scan input signals (col. 2, lines 60-67), providing boundary scan output signals (col. 2, lines 60-67), providing signals to the chip not having a boundary scan structure (col. 3, lines 3-24), and receiving signals from the chip not having a boundary scan structure (col. 3, lines 3-24).

As per claim 10, Lulla discloses the method wherein the step of providing signals to the chip not having a boundary scan structure comprises providing commands indicate one of a plurality of operations be performed (e.g. col. 4, lines 25-67; col. 5, lines 1-7).

As per claim 11, Lulla discloses wherein the step of providing signals to the chip not having a boundary scan structure further comprises providing an address to the chip not having a boundary scan structure. See col. 5, lines 24 et seq.

As per claim 12, Lulla discloses wherein the step of providing signals to the chip not having a boundary scan structure further comprises providing data to the chip not having a boundary scan structure. See col. 5, lines 24 et seq.

As per claim 13, Lulla discloses wherein the step of receiving signals from the chip not having a boundary scan structure comprises receiving data from the chip not having a boundary scan structure addressed by some of the signals provided in the step of providing signals to the chip not having a boundary scan structure. E.g. see col. 5, lines 24 et seq.

As per claim 14, Lulla discloses a method of configuring a non-JTAG chip from a JTAG-compliant chip having core logic, the method comprising the steps of: a. loading an instruction into a JTAG TAP interface of the JTAG-compliant chip that causes the JTAG TAP interface to enable a path for serial data go from a JTAG-compliant TDI pin to the core logic of the JTAG-compliant chip (e.g. col. 7, lines 38-46; col. 3, lines 21-24);

b. defining a shift register in the core logic of the JTAG-compliant chip that receives data transferred from the TDI pin (e.g. col. 4, lines 10 et seq.); and

c. defining a controller that receives the shift register data in parallel and generates from this data signals applied to pins of the JTAG-compliant chip that are connected to pins of the non-JTAG chip (e.g. col. 4, line 62 to col. 7, line 56).

As per claim 15, Lulla discloses wherein the shift register defined in the core logic of the JTAG-compliant chip outputs data to a JTAG-compliant TDO pin. E.g. see col. 2, lines 60-67.

As per claim 16, Lulla discloses the additional step performed by the controller of receiving signals from the non-JTAG chip. E.g. col. 6, lines 47 et seq.

As per claim 17, Lulla discloses wherein the shift register comprises two shift registers, one of which receives address data addressing part of the non-JTAG chip and another of which receives data words for being loaded into the non-JTAG chip. E.g. see col. 7, lines 38-46.

As per claim 18, Lulla discloses wherein the shift register receives both address data for addressing part of the non-JTAG chip and data words for being loaded into the non-JTAG chip. E.g. See col. 5, line 8 to col. 7, line 37.

As pre claim 19, Lulla discloses wherein the address data is loaded into the shift register first, and becomes a starting address for subsequent data words to be loaded into the non-JTAG chip, and is incremented internally by the controller for loading a plurality of the data words. E.g. See col. 5, line 8 to col. 7, line 37.

As per claim 20, Lulla discloses wherein the address data, data word, and any other data needed by the non-JTAG chip are applied in parallel to the non-JTAG chip. E.g. See col. 5, line 8 to col. 7, line 37.

As per claim 21, Lulla discloses wherein the address data, data word, and any other data needed by the non-JTAG chip configure part the non-JTAG chip. E.g. See col. 5, line 8 to col. 7, line 37 and col. 7, line 56 to col. 9, line 35.

## *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeppesen, III et al. (USPN 5,708,773; Jeppesen) in view of Tomita (USPN 6,324,096).

As per claim 7, Jeppesen teaches the claimed invention as detailed supra except for using the controller to program or erase the flash memory chip. Tomita teaches that it is known at the time the invention was made to use the JTAG technology to program or erase the flash memory chip. It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the JTAG technology to program or erase the flash memory chip as taught by Tomita in the system of Jeppesen since Tomita states that it would be convenient if the same interface could also be used to program flash memory in the chip so that debugging and reprogramming could be carried out in the same environment simply by connecting a debugger and programmer device to the test access port, without the need for special equipment or wiring.

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached form PTO-892.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to XUAN M. THAI whose telephone number is 703-308-2064. The examiner can normally be reached on Monday to Friday from 8:30 A.M. to 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

XUAN M. THAI
Primary Examiner
Art Unit 2111

XMT